WE CLAIM:

1. Apparatus for processing data, said apparatus comprising:

a memory operable to store data values; and

memory accessing logic responsive to memory access instructions to access data values stored within said memory; wherein

said memory has a first memory address region and a second memory address region;

said memory accessing logic is operable, in response to a memory access instruction specifying a first memory access to a first data value within said first memory address region, to convert said first memory access to a second memory access, said second memory access being to a second data value within said second memory address region;

when said first memory access is a memory write, said second memory access is a read-modify-write memory access in which Y bits within said first data value are written to Y bits within said second data value with those bits within said second data value other than said Y bits being unaltered; and

when said first memory access is a memory read, said second memory access is a masked read memory access in which Y bits of said first data value are read from Y bits of said second data value and those bits within said first data value other than said Y bits are set to a predetermined value independent of bits of said second data value other than said Y bits.

2. Apparatus as claimed in claim 1, wherein Y is a user programmable value.

3. Apparatus as claimed in claim 1, wherein Y is between 1 and 8.

4. Apparatus as claimed in claim 1, wherein said first data value is an N-bit data value and N is one of 32, 16 and 8.

5. Apparatus as claimed in claim 1, wherein said second data value is an M-bit data value and M is one of 32, 16 and 8.

6. Apparatus as claimed in claim 1, wherein said first memory address region and said second memory address region map to common physical memory storage circuits.

7. Apparatus as claimed in claim 1, wherein said Y bits are contiguous bits within said first data value.

8. Apparatus as claimed in claim 1, wherein said Y bits are a least significant Y bits of said first data value.

9. Apparatus as claimed in claim 1, wherein said memory is byte addressable and Y is less than 8.

10. Apparatus as claimed in claim 1, wherein said read-modify-write memory access is performed as an atomic read-modify-write memory access.

11. Apparatus as claimed in claim 1, wherein if said first memory access is unaligned, then said second memory access is realigned.

12. A method of processing data, said method comprising the steps of:

storing data values within a memory; and

in response to memory access instructions, accessing data values stored within said memory; wherein

said memory has a first memory address region and a second memory address region;

in response to a memory access instruction specifying a first memory access to a first data value within said first memory address region, converting said first memory access to a second memory access, said second memory access being to a second data value within said second memory address region;

when said first memory access is a memory write, said second memory access is a read-modify-write memory access in which Y bits within said first data value are written to Y bits within said second data value with those bits within said second data value other than said Y bits being unaltered; and

when said first memory access is a memory read, said second memory access is a masked read memory access in which Y bits of said first data value are read from Y bits of said second data value and those bits within said first data value other than said Y bits are set to a predetermined value independent of bits of said second data value other than said Y bits.

13. A method as claimed in claim 12, wherein Y is a user programmable value.

14. A method as claimed in claim 12, wherein Y is between 1 and 8.

15. A method as claimed in claim 12, wherein said first data value is an N-bit data value and N is one of 32, 16 and 8.

16. A method as claimed in claim 12, wherein said second data value is an M-bit data value and M is one of 32, 16 and 8.

17. A method as claimed in claim 12, wherein said first memory address region and said second memory address region map to common physical memory storage circuits.

18. A method as claimed in claim 12, wherein said Y bits are contiguous bits within said first data value.

19. A method as claimed in claim 12, wherein said Y bits are a least significant Y bits of said first data value.

20. A method as claimed in claim 12, wherein said memory is byte addressable and Y is less than 8.

21. A method as claimed in claim 12, wherein said read-modify-write memory access is performed as an atomic read-modify-write memory access.

22. A method as claimed in claim 12, wherein if said first memory access is unaligned, then said second memory access is realigned.